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		Application Number	TBD
		Filing Date	11/01/01
		First Named Inventor	Robert H. Havemann
		Group Art Unit	TBD
		Examiner Name	TBD
Attorney Docket No. <b>TI-27506</b>			

1046 U/001472  
1046 U/001472

## **U.S. PATENT DOCUMENTS**

Exam. Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
	AA					
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## FOREIGN PATENT DOCUMENTS

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#### OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Exam. Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
EDJ	CA	Zielinski et al, "Damascene Integration of Copper and Ultra-Low-k Xerogel for High Performance Interconnects," IEDM 97, pp. 936-938.	
	CB	Lee et al., "Application of HSQ (Hydrogen Silsesquioxane) Based SOG to Pre-Metal Dielectric Planarization in STC (Stacked Capacitor) DRAM," 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 112-113.	
	CC	List et al, "Integration of Ultra-Low-k Xerogel Gapfill Dielectric for High Performance Sub-0.18 $\mu$ m Interconnects," 1997 Symposium on VLSI Technology Digest of Technical Papers, pp. 77-78.	
EDJ	CD	Jeng, et al., "Process Integration and Manufacturability Issues for High Performance Multilevel Interconnect," Mat. Res. Soc. Symp. Proc., Vol. 337, pp. 25-31.	
	CE		
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